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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/090,829	03/06/2002	Alexander Roger Deas	2002	5803

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RANDALL E MURPHY
P.O Box 633334
Nacogdoches, TX 75963

EXAMINER	
NGUYEN, BINH QUOC	

ART UNIT	PAPER NUMBER
2664	

DATE MAILED: 12/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/090,829	DEAS ET AL.	
	Examiner	Art Unit	
	Binh Q. Nguyen	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/04/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. **Claims 6, and 10** are objected to because of the following informalities:

Regarding claims 18, and 21; "The method" on line 2 of claim 6, must be changed to -- A method--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> **(b)** the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims **1-24** are rejected under 35 U.S.C. 102(b) as being anticipated by ***Sekino*** the US Patent No: (US 5,22,775).

Regarding claim 1; ***Sekino*** teaches an interface device *(see Fig. 2, item "81 IC Connecting Board" means an interface device)* for connecting a transmitting device *(see Fig. 2, and 3, item "10 Tester Main Body" means a transmitting device)* having a first plurality of terminals *(see Fig. 2, items " X1,...Xn I/O Term" mean a first plurality of terminals)* and deriving a plurality of signals of a predetermined data pattern *(col. 8, line 58-to-col. 9, line 29)*, the signals being arranged in groups *(see Fig. 2, each " X1,...Xn I/O Term" are deriving a plurality of signals of a predetermined data pattern, the signals being arranged in groups)*, and

a receiving device *(see Fig. 2, and 3, item "1 IC" means a receiving device)* having a second plurality of terminals for receiving said signals *(see Fig. 2, item "1 IC" have PIN P1, ... Pn which means a second plurality of terminals for receiving said signals)*;

the interface device comprising:

input connectors *(see Fig. 2, items "L1(T1),...Ln(Tn) at the right end connecting to item 82" mean input connectors)* connectable to said transmitter's terminals *(see Fig. 2, items " X1,...Xn I/O Term" mean said transmitter's terminals)* and output connectors *(see Fig. 2, item " IC socket 82" which has plurality sockets to connect P1,...Pn, means output connectors)* connectable to said receiver's terminals *(see Fig. 2, items "P1,...Pn" mean said receiver's terminals)*;

a plurality of transmission lines *(see Fig. 2, items "L1(T1),...Ln(Tn)" mean a plurality of transmission lines)* within said interface device *(see Fig. 2, item "81 IC Connecting Board" means an interface device)*, for interconnecting said input and output connectors, the transmission lines being arranged in groups corresponding to said groups of signals *(see col. 5, lines 30-39)*; and

a nonvolatile memory *(see Fig. 2, items "83 MEM (NON-VOLATILE)" means a nonvolatile memory)* for storing data on timing errors in each said group of transmission lines *(see col. 10, lines 28-67)*, measured with respect to a reference signal and relating to a specific data pattern *(see col. 5, line 61-to-col. 6, lines 20)*;

wherein the transmitting device is capable of compensating for timing errors in said groups of transmission lines using data read from said nonvolatile memory *(see col. 7, lines 31-61)*.

Regarding claim 2. ***Sekino*** teaches the interface device of claim 1, wherein said transmission lines in one group are of equal electrical length *(see col. 1, line 60-66).*

Regarding claim 3. ***Sekino*** teaches the interface device of claim 1, wherein, in case the transmitting device comprises a plurality of registers for driving signals *(see Fig. 2, col. 4, lines 14-31, items " skew adjusting data registers 66A and 66B" means a plurality of registers),* each register having a respective delay vernier for controlling a separate group of signals, the signals controlled by a separate vernier are fed to a separate group of input connectors *(see col. 8, line 58-to-col. 9, line 29).*

Regarding claim 4. ***Sekino*** teaches the interface device of claim 1, wherein the data stored in said non-volatile memory comprises data on crosstalk timing errors measured for said groups of signals *(see col. 5, line 61-to-col. 6, lines 20).*

Regarding claim 5. ***Sekino*** teaches the interface device of claim 1, wherein the data stored in said memory comprises data on crosstalk timing errors measured for each signal of the group *(see col. 5, line 40-to-col. 6, lines 20).*

Regarding claim 6. ***Sekino*** teaches the interface device of claim 1, wherein the data stored in said non-volatile memory comprises data on interconnections between said first and second

plurality of terminals and data on crosstalk timing errors in said transmission lines relating to a specific data pattern, for each of said stored interconnection *(see col. 5, line 61-to-col. 6, lines 64)*.

Regarding claim 7. ***Sekino*** teaches the interface device of claim 1, wherein the data stored in said non-volatile memory comprises data measured in a series of iterations *(see col. 9, lines 26-29)*.

Regarding claim 8. ***Sekino*** teaches the interface device of claim 1, wherein the data are stored in the form of a table containing update values entered during each iteration for centering said groups of signals with respect to the reference signal *(see col. 1, lines 26-44)*.

Regarding claim 9. ***Sekino*** teaches a semiconductor device test system *(see col. 1. lines 5-10)* having a plurality of terminals *(see Fig. 2, items " X1,...Xn I/O Term" mean a plurality of terminals)* and deriving a plurality of signals of a predetermined data pattern *(col. 8, line 58-to-col. 9, line 29)*, the signals being arranged in groups *(see Fig. 2, each " X1,...Xn I/O Term" are deriving a plurality of signals of a predetermined data pattern, the signals being arranged in groups)*, to be applied to a semiconductor device under test *(see Fig. 2, item "1 IC" means a semiconductor device under test)* , the test system comprising an interface device for connecting the test system and the semiconductor device *(see Fig. 2, item "81 IC Connecting Board" means an interface device)*; the interface device comprising:

input connectors *(see Fig. 2, items "L1(T1),...Ln(Tn) at the right end connecting to item 82" mean input connectors)* for connecting to said terminals of the test system *(see Fig. 2, items "X1,...Xn I/O Term" mean said terminals of the test system)* and output connectors *(see Fig. 2, item " IC socket 82" which has plurality sockets to connect P1,...Pn, means output connectors)* for connecting to said semiconductor device terminals *(see Fig. 2, items "1 IC has PIN P1,...Pn" mean said semiconductor terminals)*;

a plurality of transmission lines *(see Fig. 2, items "L1(T1),...Ln(Tn)" mean a plurality of transmission lines)* within said interface device *(see Fig. 2, item "81 IC Connecting Board" means said interface device)*, the transmission lines being arranged in groups corresponding to said groups of signals*(see col. 5, lines 30-39)*; and

a nonvolatile memory *(see Fig. 2, items "83 MEM (NON-VOLATILE)" means a nonvolatile)* for storing data on interconnections between said input and output connectors *(see col. 10, lines 28-67)*and data on timing errors in each said group of transmission lines measured with respect to a reference signal and relating to a specific data pattern, for each of said stored interconnection *(see col. 5, line 61-to-col. 6, lines 20)*;

wherein the test system is capable of compensating for timing errors in said groups of transmission lines using data read from said nonvolatile memory *(see col. 7, lines 31-61)*.

Regarding claim 10. ***Sekino*** teaches the system of claim 9, wherein said transmission lines of one group are of equal electrical length *(see col. 1, line 60-66)*.

Regarding claim 11. ***Sekino*** teaches the system of claim 9, wherein said transmission lines of one group are located within one layer of the interface device *(see col. 8, line 29-57)*.

Regarding claim 12. ***Sekino*** teaches the system of claim 9, wherein the transmitting device comprises a plurality of registers for driving signals *(see Fig. 2, col. 4, lines 14-31, items " skew adjusting data registers 66A and 66B" means a plurality of registers)*, each register having a respective delay vernier for controlling a separate group of signals, and the signals controlled by separate verniers are fed to a separate group of transmission lines *(see col. 8, line 58-to-col. 9, line 29)*.

Regarding claim 13. ***Sekino*** teaches the system of claim 9, wherein the transmitting device comprises a plurality of pin cards *(see Fig. 2, item " IC socket 82" which has plurality sockets to connect P1,...Pn, means a plurality of pin cards)* comprising registers for driving signals *(see Fig. 2, col. 4, lines 14-31, items " skew adjusting data registers 66A and 66B" means registers)*, each register having a respective delay vernier, and the signals derived from the separate pin card are fed to a separate group of transmission lines *(see col. 8, line 58-to-col. 9, line 29)*.

Regarding claim 14. ***Sekino*** teaches the system of claim 9, wherein data from crosstalk timing errors are stored with circuit connectivity data in the said nonvolatile memory in the form of a table containing update values entered during current iteration *(see col. 6, lines 21-64)*.

Regarding claim 15. ***Sekino*** teaches the system of claim 13, wherein each pin card further comprises a non-volatile memory *(see Fig. 2, items "83 MEM (NON-VOLATILE)" means a nonvolatile)* for storing data on crosstalk timing errors in the said pin card *(see col. 10, lines 28-67)*, the test system being capable of compensating for timing errors caused by crosstalk using data read from said nonvolatile memory *(see col. 5, line 61-to-col. 6, lines 20)*.

Regarding claim 16. ***Sekino*** teaches the system of claim 9, wherein the transmitter further comprises a non-volatile memory *(see Fig. 2, items "83 MEM (NON-VOLATILE)" means a nonvolatile)* for storing data on crosstalk timing errors in a tester's header *(see Fig. 2, and 3, item "10 Tester Main Body" means a tester's header)*, the test system being capable of compensating for timing errors caused by crosstalk using data read from said nonvolatile memory *(see col. 7, lines 31-61)*.

Regarding claim 17. ***Sekino*** teaches a method of compensating timing errors in transmission lines comprising the steps of:

transmitting via transmission lines *(see Fig. 2, items "L1(T1),...Ln(Tn)" mean a plurality of transmission lines)* a plurality of signals of a predetermined data pattern *(col. 8, line 58-to-col. 9, line 29)*,to be applied to a semiconductor device , the signals being driven in groups *(see Fig. 2, items "1 IC has PIN P1,...Pn" mean said semiconductor device)*;

comparing the output response of a group of signals with a reference signal level *(see col. 8, lines 29-57)*;

storing *(see col. 10, lines 28-67)* in a non-volatile memory *(see Fig. 2, items "83 MEM (NON-VOLATILE)" means a non-volatile memory)* data on timing errors in said transmission lines relating to specific data patterns, for each separate group of signals*(see col. 5, line 61-to-col. 6, lines 20)*; and

compensating for timing errors in said transmission lines for each said group of signals using said data read from nonvolatile memory *(see col. 7, lines 31-61)*.

Regarding claim 18. ***Sekino*** teaches the method of claim 17, wherein the procedure of compensation timing errors is iterative *(see col. 6, lines 21-64)*.

Regarding claim 19. ***Sekino*** teaches the method of claim 18, wherein, during the first iteration, the timing errors are measured for groups of signals, each group of signals being controlled by a separate delay vernier of a transmitter's register *(see col. 8, line 58-to-col. 9, line 29)*.

Regarding claim 20. ***Sekino*** teaches the method of claim 18, wherein, during the first iteration, the timing errors are measured for groups of signals, each group of signals relating to a separate pin card *(see col. 8, line 58-to-col. 9, line 29)*.

Regarding claim 21. ***Sekino*** teaches the method of claim 17, wherein, for each group of signals, the leftmost and the rightmost skew value with respect to a reference signal are measured and the whole group of signals is shifted for the average of these two values to adjust its position with respect to the reference signal *(see col. 7, line 63-to-col. 8, line 5)*.

Regarding claim 22. ***Sekino*** teaches the method of claim 17, wherein the timing errors are measured for each bit of a signal *(see col. 5, line 40-to-col. 6, line 20)*.

Regarding claim 23. ***Sekino*** teaches the method of claim 17, wherein, before skew measurements, a clock signal delay is measured to provide high accuracy in subsequent measurements *(see col. 5, line 61-to-col. 6, line 20)*.

Regarding claim 24. ***Sekino*** teaches a method of testing a semiconductor device comprising

transmitting via transmission lines*(see Fig. 2, items "L1(T1),...Ln(Tn)" mean transmission lines)* a plurality of signals of a predetermined data pattern *(see col. 5, lines 30-39)* to be applied to said semiconductor device, the signals being arranged in groups *(see Fig. 2, items "1 IC has PIN P1,...Pn" mean said semiconductor device)*;

comparing the output response of a group of signals with a reference voltage *(see col. 8, lines 29-57)*;

storing *(see col. 10, lines 28-67)* in a non-volatile memory *(see Fig. 2, items "83 MEM (NON-VOLATILE)" means a non-volatile memory)* data from crosstalk artifacts in said transmission lines relating to specific data patterns, for each separate group of signals *(see col. 5, line 61-to-col. 6, lines 20)*; and

compensating for artifacts caused by crosstalk in said transmission lines for each said group of signals using said data read from said nonvolatile memory *(see col. 4, lines 14-31, and col. 7, lines 31-61)*.

Contact Information

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh Q. Nguyen whose telephone number is 571-272-8563. The examiner can normally be reached on M-F: 9:00 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on 571-272-3134. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Respectfully submitted,

By:
Binh Q. Nguyen
Patent Examiner
12/22/2005

Ajit Patel
Primary Examiner